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EXAMINER
THOMAS, TOM

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,145	NOGAMI ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *October 9, 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Cancellations

1. Applicant's cancellation of Claim 10 in Letter No. 13 of June 10, 2003 is acknowledged.

Claim Rejections – 35 U.S.C. 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. (US 6,259,160 B1) in view of Dubin et al. (US 5,695,810), Shacham-Diamand ("High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," Proc. Materials for Advanced Metallization Workshop (Europe) (1997) pp. 11-14) and Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits," Noyes Publ., Westwood, New Jersey (1993), p. 44, 428)

Lopatin et al. disclose a structure containing a barrier liner material (TaN) filled with copper (40,41) (See Figure 1). After subsequent deposition of a copper plug atop the first interconnect, a CoWP layer (60) (See Figure 4) is formed (Col. 7, lines 47 – 48) around the copper as an oxidation resistant layer. A similar CoWP "barrier" layer depos-

ited on copper is disclosed by Dubin et al. (Col. 9, lines 57 – 62) as part of a copper interconnect structure on a semiconductor wafer (Col.9, lines 46 – 47). Lopatin et al. do not disclose the formation of a cobalt silicide cladding layer by CVD on the surface of the CoWP layer. However, Shacham-Diamand et al. disclose the electroless deposition

of copper, followed by electroless deposition of CoWP with deposited films of Co and Si atop the CoWP to produce the sequence, Cu/CoWP/Co/Si, which was subsequently subjected to annealing at 400 degrees (C) for 30 minutes to one hour. The results indicated no interdiffusion and no significant change in resistivity, reducing the affinity for oxidation and corrosion. However, it is also notoriously well known that cobalt silicide is formed from Co/Si at a temperature of 400 degrees (C) (Wilson et al., Table 1, p.44). Hence, it is inherently known that a cobalt silicide layer is formed on the CoWP after annealing. Further, the presence of an oxygen containing layer atop the clad layer is not disclosed by Lopatin et al. However, oxygen containing layers (oxides) on metal layers in interconnect structures is notoriously well known (See for example, Wilson, p. 428). It would have then been obvious to one of ordinary skill in the art at the time of the invention to combine the resulting Cu/CoWP/CoSi structure of Shacham-Diamand (1997) with Lopatin et al., Dubin et al., and Wilson et al. to produce a stable structure as a diffusion barrier for copper (plugs and interconnect lines) and outer clad layer (CoWP) resistant to chemical reaction, interdiffusion and oxidation.

4. Claims 5 - 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Lopatin et al. (US 6,259,160 B1) in view of Dubin et al. (US 5,695,810), Shacham-Diamand and Wilson et al.

5. Regarding Claims 5, 7, and 11, Lopatin et al. disclose a structure containing a barrier liner material (TaN) filled with copper (40,41) (See Figure 1). After subsequent deposition of a copper plug atop the first interconnect, a CoWP layer (60) (See Figure 4) is formed (Col. 7, lines 47 – 48) around the copper as an oxidation resistant layer. A similar CoWP "barrier" layer deposited on copper is disclosed by Dubin et al. (Col. 9, lines 57 – 62) as part of a copper interconnect structure on a semiconductor wafer (Col.9, lines 46 – 47). Lopatin et al. do not disclose the formation of a cobalt silicide cladding layer by CVD in a single step on the surface of the CoWP layer. However, Shacham-Diamand et al. disclose the electro- less deposition of copper, followed by electroless deposition of CoWP with deposited films of Co and Si atop the CoWP to produce the sequence, Cu/CoWP/Co/Si, which is subsequently subjected to annealing at 400 degrees (C) for 30 minutes to one hour. The results indicated no interdiffusion and no significant change in resistivity, reducing the affinity for oxidation and corrosion. However, it is also notoriously well known that cobalt silicide is formed from Co/Si at a temperature of 400 degrees (C) (Wilson et al., Table 1, p.44). Hence, it is inherently known that a cobalt silicide layer is formed on the CoWP after annealing. The formation of a cobalt silicide layer by a two-step process (deposition plus anneal) as contrasted to a single step CVD process produces the same result and a functional working device and is therefore obvious. It has been ruled by the court that the performance of two steps simultaneously which have previously been performed in sequence is a case of obviousness. In re Tatincloux, 108 USPQ 125 (CCPA

1955).

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. in view of Dubin et al. (US 5,695,810), Shacham-Diamand and Wilson et al., as applied to Claims 5 – 7, and 11, and further in view of Sherman ("Chemical Vapor Deposition for Microelectronics," Noyes Publ., Westwood, New Jersey, (1987) pp. 66 – 67).
Lopatin et al. do not disclose the formation of a silicon oxide by adding oxygen to silane In a reaction process. However, the formation of silicon oxide on a semiconductor surface using a mixture of silane and oxygen in a reaction process has been utilized for over two decades and is notoriously well known in the art (See for example, Sherman, p. 67,1st par.) Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Dubin et al., Shacham-Diamand, Wilson et al., and Lopatin et al. to obtain a silicon oxide layer formed by an oxygen/silane reaction for use as a passivation or scratch protection layer (p. 66, 2nd par).

7. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. in view of Dubin et al., Shacham-Diamand, Wilson et al., and Sherman. Lopatin et al. disclose a device containing a barrier liner material (TaN) filled with copper (40,41) (See Figure 1). After subsequent deposition of a copper plug atop the first interconnect, a CoWP layer (60) (See Figure 4) is formed (Col. 7, lines 47 – 48) around the copper as an oxidation resistant layer. A similar CoWP "barrier" layer deposited on copper is disclosed by Dubin et al. (Col. 9, lines 57 – 62) as part of a copper

interconnect structure on a semiconductor wafer (Col.9, lines 46 – 47). Lopatin et al. do not disclose the formation of a cobalt silicide cladding layer by CVD on the surface of the CoWP layer. However, Shacham-Diamand et al. disclose the electroless deposition of copper, followed by electroless deposition of CoWP with deposited films of Co and Si atop the CoWP to produce the sequence, Cu/CoWP/Co/Si, which was subsequently subjected to annealing at 400 degrees (C) for 30 minutes to one hour. The results indicated no interdiffusion and no significant change in resistivity, reducing the affinity for oxidation and corrosion. However, it is also notoriously well known that cobalt silicide is formed from Co/Si at a temperature of 400 degrees (C) (Wilson et al., Table 1, p.44). Hence, it is inherently known that a cobalt silicide layer is formed on the CoWP after annealing.

Lopatin et al. do not disclose the direct formation of a silicon oxide on the cobalt silicide surface. However, the formation of silicon oxide on a semiconductor surface using a mixture of silane and oxygen in a reaction process has been utilized for over two decades and is notoriously well known in the art (See for example, Sherman, p. 67,1st par.). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Dubin et al., Shacham-Diamand, Wilson et al., and Lopatin et al. to obtain a silicon oxide layer formed by an oxygen/silane reaction for use as a passivation or scratch protection layer (p. 66, 2nd par).

Response to Arguments

8. Arguments of Applicant have been carefully considered but have not been found to be persuasive. The prior art clearly shows the claimed invention recited in the instant application, including formation of a clad layer. The oxide atop the clad layer is notoriously well known in the art, and commonly used in interconnect structures.

Conclusions

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305-5396**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner are unsuccessful, the examiner's supervisor, **Tom Thomas**, can be reached on **(703) 308-2772**. The fax number for the organization where this application or proceeding is assigned is **(703) 308-7722**.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
June 27, 2003